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# REVIEW OF COMPOUND SEMICONDUCTORS RELIEVING BOTTLENECKS OF INCESSANT MOSFET SCALING: HEROISM OR A RACE IN THE DARK

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**Abstract:** In last five decades, the exponential demand in the field of electronic applications is powered by a drastic escalation in the compactness of silicon based complementary metal oxide semiconductor (CMOS) field effect transistor (FETs) and qugumentation in logical performance. But silicon based transistor scaling is now heading to its restraints, intimidating to cease the micro-electronics revolution. Another family of semiconductor materials thus have been under surveil- lance that can be rightly placed to handle this problem: Compound Semiconductors. The spectacular electron transport features of such materials might be point of focus that can lead to development of FETs based on such materials in nano-scale regime. This article provides a speculation in the future of compound semiconductor material-based devices with emphasis on effects of incessant scaling. Whilst aggressive scaling, requirements and constraints that include power dissipation, operating frequency, gain, leakage current must be kept balanced with predictive technologies nodes and also with the fabricating aspects of devices. The scaling restraints requisite a transformation from planar architectures to three-dimensional device structures to cater future performance requirements of CMOS nodes beyond 10 nm. Compound semiconductor materials are progressively waged in various electronic, opto-electronic, and photonic applications due to the prospects of adjusting the properties over a broad parameter domain conveniently by tuning the alloy composition. Ironically, the material properties are also willed by the atomic-scale orientation of compound semiconductors in sub-nanometer scale. Compound semiconductors FET based logic circuits perform 5 folds faster than similar topology circuits based on silicon, whilst dissipating only half of the power. Here a comprehensive review is presented that outlines how compound semiconductor materials mitigate various effects of aggressive scaling in nanometer scale and the adjoining effects.

**Keywords:** *Compound Semiconductors; RF Performance; Scaling; Field Effect Transistors; High Electron Mobility Transistors.*

## 1. Introduction

The The revolution of microelectronics may be best reflected through ‘smaller the better’. The indistinct feature of silicon metal-oxide-semiconductor field-effect transistor (MOSFET), a field function, is that its cognitive properties improve as its size is reduced [1]. When it comes to the functioning of the logical concept, the transistor impersonates a switch, and the primal characteristics include the time and energy budget. Since MOSFETs have reduced in size following the geometric scaling rule, the change in speed and magnitude of the transistor density has exponentially increased, while as the switching energy have reduced in the similar manner [2]. Such ‘triple benefits’ of the

MOSFET measurement have enabled the transformation of electronics. Advanced sensible digital circuits are based on p-type and n-type configured transistors with specific characteristics popular by the name metal-oxide-semiconductor (CMOS) compatible transistors (CMOS) and have become an outstanding class of circuits owing to simpleness and distinctly power efficient characteristics allowing for the integration of very dense circuits. Two decades back, the MOSFET scaling moved into the 'power-controlled phase' as electrical power is dispersed by logic chips striking about 100Wcm [3]. Power cannot be increased continuously without being subjected to large packaging and cooling budget which renders the chips ineffective in many operating systems. The continuous constriction of the transistor leads to reduction in working voltage which adversely affects the speed of switching [4]. This problem has caused the operating voltage of CMOS transistors to be dropped to about 1V. This poses a challenge in further scaling of generic CMOS technology transistors.

One of the probable solutions is to induce a new channel material medium where charge carriers will traverse at a much higher speed as compared to silicon. This will allow for voltage reduction without any performance loss. This could be the reason for the attention turning towards compound semiconductors of III-V groups including GaAs, InAs, InP, AlAs and their ternary and quaternary alloys, include the combined elements of column III and V in the periodic table. Majority of III-V compound semiconductors have distinctive electronic and optical properties. These are mostly used in light emitting diodes, lasers, musical instruments, light communication equipment and hearing aids because of indirect energy bandgap which enables to emit and detect light. Some of these, mainly InAs, GaAs, and InGaAs show outstanding properties of electron transport mechanism. Transformers which are mainly based on such materials form the core of many high-frequency and high speed advanced electronic applications [5]. There is a gigantic and advanced industry producing III-V integrated circuits in tremendous scale for wide variety of applications ranging from smart phones, fiber-optic systems, cellular base stations, satellite communications, wireless local area networks, radars, radio astronomy and security systems. The extensive use of hand-held devices and their extensive data usage have been a bonus to the III-V circuit sector, now characterized by massive automation and bold, high-end wafers, sophisticated device design tools, well-designed device reliability, and a rich and competitive industrial system.

At present attempts are being made to replace silicon with other class of materials which can result in devices with remarkable list of attributes. III-V family of materials are receiving considerable attention from worldwide research community. In the recent past the role of compound semiconductor materials like SiGe, AlGaN, GaN have been recognized by International Technology Roadmap for Semiconductor (ITRS). Fundamentally the family of III-V CMOS is receiving attention due to extraordinarily high carrier mobility and tuning ability of energy bandgap. For similar sheet resistance, materials like InAs or InGaAs offer mobility ten times higher to silicon. The exceptionally good response of III-V material-based transistors is often the highlighted feature. It has been experimentally demonstrated for In- GaAs based high electron mobility transistors, the power and current gain exceeds 600GHz and 1THz respectively which is quite remarkable [6]. Although these features are least desired for logic applications. A logic transistor is a multi-terminal ON and OFF state switch which requires fast switching speed enabled by high ON state current. The static power dissipation is a liability created by OFF state current. The quest for development of super-fast electronic devices is driven by challenge in limited charge carrier speed in silicon which is being replace by compound materials like GaAs with significantly high charge carrier mobility within same range of applied electric fields. Beside advantage of high mobility compound semiconductor materials offer advantages desirable for logic and microwave devices that aim to operate at high frequencies finding compatibility with optical fiber transmission circuits. It has been demonstrated that FET logic circuits based on

compound semiconductors deliver three folds better performance in comparison to silicon-based circuits whilst consuming only half as much power. At nanoscale the performance is expected to improvise even better forming small quantum wells. One of the challenges in development of such transistors is that switching time is less as compared to transient time of the circuit creating serious latency issues. Hence the quest for new architectures and clocking strategies that will sync the transient and switching times. Semiconducting GaAs wafers offer flaunting bulk resistivity of 108 Ω-cm which has accompanying advantage of convenience in placing the insulating material. GaAs offers a possibility of development of single crystalline hetero-junctions and interfaces with no or minimal defects leading to formation of very little trapped charges. The hetero junctions between GaAs and AlGaN results in the formation of electron or hole gas depending on type of quantum well formation yielding charge carriers with high velocities. Compound semiconducting material are generally of wide and direct energy band gap where the incident photons can cause electron transitions irrespective of h-phonon momentum conservation finding application in photonic applications such as lasers. The listed advantages of compound semiconducting materials place them in the top tier materials for investigation in development of modern-day device and circuit applications.

Compound semiconductors have in recent times have proved to play an all important and critical role in fabrication of opto-electronics, high-density data storage systems and sensing devices. The direct bandgap electronic structure and their flexibility to create energy bandgap engineered structures are the key features that make them suitable for a wide variety of applications. The prospects for creation of hetero structures and quantum structures (e.g., quantum-wells (QWs), quantum wires, and quantum-dots (QDs)) due to energy band offsets due to lattice mismatch and ability to restrict photons and electrons (and holes) in the optoelectronic devices that leads to improved efficiency and multidimensional functionality. Such compound semiconductor based QWs and QDs have found a powerful applicability in optoelectronic devices that include lasers, photodetectors, modulators and semiconductor optical amplifiers (SOAs).

### 1.1 Critical Review

Till now the bright side that included advantages have been highlighted. The development of compound material semiconductor devices is held up by number of roadblocks and consistent efforts are being made to overcome and mitigate these limitations of unwanted effects that come along. In the general concept the limitations on the adoption of a new CMOS technology channel object are enormous. Scaling has been one of main objectives for de- vice design engineers. When the technology is ready to be deployed, the required transistor gate length might be smaller than 10nm. To meet the challenge, a disorderly technology, like incorporating III-V compounds, it will need to deliver the best performance (at least 30-50%). It should also promise to bring more than one future generation to come. It could be obtained with the least expensive manufacturing and better reliability. The alloys of the semiconductor compounds have received much attention in recent decades due to their great power for applications in electronic, optoelectronic, modulators, field effect transistors, high- speed transistors, infrared detectors, light emitting diodes and lasers and power amplifiers. Herein this article we have tried to contemplate various aspects of compound semiconductor materials and cross correlated various aspects of different devices. We have channelized our discussion in finding the answer to questions of compound semiconducting materials providing same performance as that of generic silicon-based CMOS technology for higher technology nodes.

## 2. Outlook On Compound Semiconductor Materials

Compound semiconductor material-based devices have brought a new paradigm shift in extended applications of electronic devices. Owing to the possibility of modulating the properties over a wide

range through appropriate composition factor. At nanometer scale, the atomic structural arrangement influences the material properties. Features such as interatomic spacing and bond angle tend to have a striking impact on crystallinity of a material. The inter atomic spacing has a significant impact on energy band gap and predominant effect is observed in bandgap bowing. A compound semiconductor typically takes the crystalline structure of parent crystal however there is a change in lattice constant that depend on the composition factor governed by Vegard's law. The tiny linear change with composition factor that accounts to about 10% to 30% of that likely from the change in lattice constants. Specifically, strong directional displacements are ascertained for the atoms occupying the common sub lattice while the atoms of the mixed sub lattice exhibit tiny and extreme isotropic spatial variations. The varied atomic layout arrangements depend on the type of atoms participating in compound material which brings to the conclusion that for a compound semiconductor material the electrical properties are predominantly affected by the structural inhomogeneity especially in the deep nanoscale regime even if computational imperfections are absent. Here in this paper, we have restricted our discussion to electrical properties of compound semiconductor materials and devices, so the discussion on material and structural properties will be out of the scope of this paper. The properties of different material and comparative values based on experimental literature is given in Table 2. The discussion for different compound semiconductor material is given below:

### 2.1 Silicon Germanium (Si(1−x)Gex)

One of the main aspects of SiGe material in comparison to generic silicon is its lower adjustable energy band gap controlling it by germanium content also called as mole fraction [7]. For SiGe compound material, the energy bandgap (EG) reduces by about 75eV for every 10% of Ge introduced in Si. For Si(1−x) Ge(x) with "x" as mole fraction parameters such as electron and hole mobility (μn, μp) and respective saturation velocities are function of mole fraction "x", in accordance with equations given in Table 1. From fabrication perspective SiGe is the most convenient to replace Si as it can be processed with same process line as employed for generic CMOS technology. Another advantage of SiGe over III-V compound semiconductors like GaAs includes its native oxide formation required for MOS structures which lacks in later. Also, GaAs wafer suffers from issues of mechanical fragility which limits the wafer size. SiGe BiCMOS technology has outperformed the classical CMOS technology in terms of offering better frequency response, noise figure and linearity. The SiGe BiCMOS technology provides higher performance figure of metrics. More ever SiGe bipolar technology if combined with modern day CMOS technology and wide range of passive devices indispensable for realization of integrated mixed-signal system-on-a-chip (SoC).

Table 1: Equations for computing mobility ($\mu$) and saturation velocity ($v_{sat}$) for different mole fractions (x) in vsat in Si(1−x)Ge(x).

| References | Modeling Equations of $\mu$ and $v_{sat}$ in $Si_{(1-x)}Ge_{(x)}$ |
|---|---|
| [8] | $\mu_n$, Si(1-x) Ge(x)= $e^{(7.37-10.9x+11.5x^2)}$ |
| [8] | $\mu_{P,}$ $Si_{(1-x)}Ge_{(x)} = e^{(6.35-5.97x+6.97x^2)}$ |
| [9] | $V_{sat, n,}$ $Si_{(1-x)}$ $Ge_{(x)}$ = $((0.98+2.93x-2.3x^2)10^{-7})^{-1}$ |
| [9] | $V_{sat, p,}$ $Si_{(1-x)}Ge_{(x)}$ = $(1.36+1.91x-1.88x^2)^{10-7})^{-1}$ |

### 2.2 Gallium Nitride (GaN)

GaN till date has been the strongest counterpart contender technology in space applications where energy efficacy is a parameter of paramount importance. GaN is not characterized by highest carrier mobility however comparable maximum frequency of operations besides advantages of high-power density and efficacy make it a promising candidate in power MOS- FETs. Due to high output

impedance of GaN based transistors, which renders to ease in designing of cascaded amplifiers. GaN as a material find wide range variants in MOSFETs that include bipolar junction transistors (BJTs), E-mode MOSFET, MESFET, high electron mobility transistor, FinFETs, and LDMOS. Imperatives of the performance requirements the above listed MOSFET versions find specific applications due to versatile features discussed latter in this paper. For automotive applications, GaN owing to its wide energy bandgap finds use in high-power microwave devices. It has been observed that GaN based devices have operated well at temperature of about 320◦C showing the capability of high temperature operations. GaN HEMTs show distinguished feature of formation of two dimensional gas (2DEG) induced as a result of spontaneous polarization and lattice mismatch of bulk and epitaxial layer. The polarization charges is also supported by piezoelectricity of GaN material. The most common cap layer to induce 2DEG is another compound semiconductor material AlGaN.

### 2.3 Silicon Carbide (SiC)

SiC is the best competitor of GaN even though its power density is not higher than that of GaN, it procures other features like high thermal conductivity enabling its application in variety if semiconductor devices. Schottky barrier (SB) MOSFETs based on SiC have estab- lished their presence and replaced almost Si based SB-MOSFETs owing to high voltages and power handling capabilities. SiC and counterpart GaN showcase the potential trade-off be- tween high switching speeds, high-voltage blocking capability, high-temperature operation, manufacturing availability and technology convenience [10]. Sufficiently high breakdown electric field of SiC tends to have thin and high doping of blocking layers. SiC is attributed by other advantages that include wide energy bandgap at high temperatures and radiation hardened device besides having high thermal conductivity that extracts the device heat [11]. SiC has been employed for simpler junction field effect transistors like normally-ON JFET cascaded with low power Si-MOSFET [12].

### 2.4 Gallium Arsenide (GaAs)

GaAs is characterized by wide energy bandgap, sufficiently high mobility and high operating frequency besides inherently being radiation hardened material. GaAs displays extremely efficiently qualities for conversion of radiation energy to electrical equivalent along with being radiation hardened finds tremendous applicability in devices used for military and space applications that require solar power. GaAs material-based technologies are looking to dominate the semiconductor device production market; however, Si still being preferred due to well established process besides its availability abundance and cost efficacious. GaAs in comparison to Si is attributed by wide energy bandgap and high drift velocity pertaining to high mobility. However, GaAs suffers process complexity in comparison to Si as it is often encountered by crystal defects. GaAs and Si devices do not match perfectly with each other hence making this process cost ineffective to deposit GaAs over Si [13].

### 2.5 Indium Phosphate (InP)

Communication systems capable of transmitting data in multi terabytes per second require in chip semiconductor devices that can process high speed analog and digital operations. InP, if alloyed with InGaAs, results in fast speed opto electronic circuits, capable of multiplexed functioning as photodetector, waveguides and very high-speed active class of circuits forming a complete system on chip. At the outset primarily due to direct energy bandgap of InP based devices have potential to be integrated with photonic devices in the optical wavelength band of 1.3μm to 1.55μm. InP-based heterojunction bipolar transistors functionally hold vertical MBE device profile, exhibits small surface recombination and low flicker noise. Such devices find suitability in circuits characterized by low phase jitter and enhanced receiver characteristics. InP based hetero junction bipolar transistors are

emphasized for technologies requiring low power consumption than GaAs. Besides the advantage include superior transconductance, integration as vertical structures and area efficiency. The three dimensional/vertical integration of InP based devices imply provides an edge over planar HEMT based structures. InP are epitaxially and lattice-matched to InGaAs for formation of PIN-structured multi-pixel photo diodes with enhanced-speed employed for infrared (IR) sensing. The limitation of InP based devices is cost ineffective and complex approach of fabrication. In [14] is demonstrated an InP based hetero junction bipolar transistor with measured fT = 400GHz and fmax = 700GHz showcasing the ability and potential of InP based technology [15].

Table 2: Material parameters for compound semiconductors

| Material | Energy bandgap (eV) | Permittivity | Electron Mobility ($cm^2/Vs$) | Breakdown Voltage | Power Density | Thermal Conductivity | $f_T$ |
|---|---|---|---|---|---|---|---|
| Silicon | 1.12eV | 11.8 | 1500$cm^2/Vs$ | 300kV/cm | 0.2W/mm | 1.5W/cmK | 20GHz |
| SiGe | 0.945eV | 13.95 | 7700$cm^2/Vs$ | 200kV/cm | 1W/mm | 0.08W/cmK | 285GHz |
| GaN | 3.49eV | 9 | 1500$cm^2/Vs$ | 3300kV/cm | 30W/mm | 1.5W/cmK | 150GHz |
| SiC | 3.25eV | 10 | 900$cm^2/Vs$ | 3500kV/cm | 10W/mm | 4.5W/cmK | 20GHz |
| InP | 1.35eV | 12.119 | 5400$cm^2/Vs$ | 500kV/cm | 1W/mm | 0.7W/cmK | 300Hz |
| GaAs | 1.42eV | 12.8 | 8500$cm^2/Vs$ | 400kV/cm | 0.5W/mm | 0.5W/cmK | 150GHz |

## 3. Device Performance of Compound Semiconductor Materials

Here in this section, we will talk about the device performance of various devices (mate- rial) from performance figure of merit perspectives. High electron mobility transistor is fundamentally a low noise figure device. It has been demonstrated by various research that HEMTs display great improvement in noise performance in 200 to 670 GHz frequency range. However, for short gate lengths the scaling is accompanied by degraded electrostatics which leads to reduced gm/Ids affecting the RF performance of device considerably. In InP based HEMTs, for gate length of 36nm, 18nm and 9nm, corresponding to effective oxide thickness of 0.8nm, 0.4nm, 0.2nm reveal exiting performance parameters of extrinsic transconductance (gm) to be 2.5mS/µm, 4.2mS/µm and 6.4mS/µm, On-current 0f 0.55mA/µm, 0.8mA/µm and 1.1mA/µm, ft of 0.70THz, 1.2THz and 2.0THz respectively. As the gate length is scaled down, an improvement in cut-off frequency is observed. An issue arises that the THz HEMTs cannot be scaled further due to number of issues. HEMTs usually consists of gate barriers under source drain/contacts which leads to high source/drain access resistance. This can be mitigated by source/drain regrowth technique so that no barriers are formed un- der contacts lowering the resistance values which consequently increases fmax and lowers fmin subsequently improve operating frequency range of the device. As gate length is scaled down, the gate barriers are thinned improving

gm but simultaneously lowering Gds and is accompanied by high leakage current hence barrier cannot be thinned beyond certain limit. One way to mitigate is the use of high-K gate dielectrics deposited via atomic layer deposition technique in the order of hew nm. This will certainly improve the transconductance as well as drain to source conductance while maintaining the operating frequency range. For fixed effective oxide thickness, the drain to source conductance degrades with scaling. FinFETs have better electrostatic integrity yielding better gm/Gds. III-V compound mate- rial based MOSFETs have reasonable chances of applicability in VLSI at the 7nm node. At 18nm LG, and 5nm of channel length in InAs based FETs, conductance was observed to be 3mS/mm. The bottom line for III-V based FET structures at ultra-scaled gate lengths, should have high-K dielectrics, reduced channel thickness, and small contact resistances to maintain electrostatic integrity. A comparison of various performance parameters between InP based HBTs and HEMTs taking scaling into consideration are listed in Table 3 [16].

Table 3: Performance metrics of various technologies for scaling of technology nodes.

| Technology | InP HBT | | | InP HEMTs | | | AlN/GaN HEMTs | | |
|---|---|---|---|---|---|---|---|---|---|
| Node (nm) | 64 | 32 | 16 | 36 | 18 | 9 | 1300 | 1000 | 150 |
| Current Density (mA/$\mu$m) | 36 | 72 | 140 | 0.55 | 0.8 | 1.1 | - | - | - |
| $f_{cut-off}$ (THz) | 1 | 1.4 | 2 | 0.7 | 1.2 | 2 | 9 Ghz | 6 GHz | 50 GHz |
| $f_{max}$ (THz) | 2 | 2.8 | 4 | 0.81 | 1.4 | 2.7 | 32 Ghz | 11 GHz | 102 GHz |

Advent of gate length scaling in HEMTs, goal should be to minimize the parasitic delays and restrict the aftermaths of small geometry effects (SCEs) in order to facilitate a superior high performance, deice at high frequencies. One of the most important factors in device design is the ratio between drawn gate length and gate to channel separation. This ratio has a significant effect on transistor performance should be sufficiently high to overcome the SCEs [17]. This is a necessary to maintain the ratio high but not the sufficient condition for high performance. Reducing the ratio leads to degradation in charge carrier concentration formed as 2D-electron gas. Additionally, to thin barriers, if a lattice matched InAlN or all- binary AlN, have lately been used to circumvent these issues. GaN-based hetero structures with thin wider bandgap barrier layers can provide high channel sheet carrier density and good gate control at the same time. In several material systems, advanced T-gate designs have been extensively exploited to produce large f cut−off and fmax values. A T-shaped gate configuration can achieve low gate resistance and parasitic gate capacitance at the same time.

For GaN HEMTs and MISHEMTs, a T-gate technique with a greatly scaled gate footprint (gate length 0f 50nm) has been investigated [18]. We in this section have compared six different technologies that include SiGe HBT, Si BJT, Si CMOS, III-V MESFET, III-V HBT, and III-V HEMT. The various performance parameters considered include Frequency Response, 1/f and Phase Noise, Broadband Noise, Linearity, Output Conductance, Transconductance/Area, Power Dissipation, CMOS Integration, IC Cost. The table categorizes the performance metrics as poor, fair, good, very good and excellent marking the relevance of each technology for various applications.

Table 4: Performance Comparison for different technologies from RF perspective.

| Performance Metric | SiGe HBT | Si BJT | Si CMOS | III-V MESFET | III-V HBT | III-V HEMT |
|---|---|---|---|---|---|---|
| Frequency Response | + | 0 | 0 | + | + + | + + |
| 1/f and Phase Noise | + + | + | - | - - | 0 | - - |
| Broadband Noise | + | 0 | 0 | + | + | + + |
| Linearity | + | + | + | + + | + | + + |
| Output Conductance | + + | + | - | - | + + | - |
| Transconductance/ Area | + + | ++ | – | - | + + | - |
| Power Dissipation | + + | + | - | - | + | 0 |
| CMOS Integration | + + | + + | * * | - - | - - | - - |
| IC Cost | 0 | 0 | + | - | - | - - |

(- -: Poor, -: Fair,0: Good, +: Very Good, + +: Excellent)

SiGe is characterized by lower bandgap as compared to silicon with relaxation of control- ling the energy bandgap by variation of germanium mole fraction. It has been observed that energy bandgap reduces approximately by 75 meV for every 10% of germanium introduced. SiGe has been extensively employed for HBTs since 1987. In 1990, a SiGe HBT through ultra-high vacuum/chemical vapor deposition (UHV/CVD) was demonstrated with cut-off frequency fT = 75GHz. SiGe based devices can be processed in same fabrication facility as that of established silicon hence advantageous as compared GaAs. Besides convenient fabrication process simplicity SiGe has a native oxide layer that doesn't suffer from mechanical fragility. Based on literature survey, the figure of merit performance comparison of various technologies based on different materials is shown Table 4. Figure 1 has been taken from global foundries highlighting features of RF perspectives of different technologies. [7] It has been observed that SiGe based hetero junction bipolar transistors deliver better frequency response, noise figure than generic Si based BJT and CMOS technologies. In comparison to GaAs technologies, SiGe based HBT devices reveal similar performance however at much lower cost than that of GaAs technology.

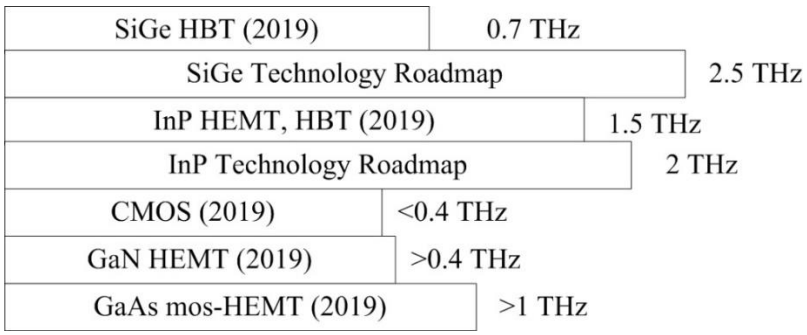


Figure 1: RF performance for THz research gap for fmax capability of various transistor technologies.

## 4. Moore's Law, Scaling, Geometry, Materials, Where to Look?

Gordon Moore proposed the famous "Moore's law" to forecast the time rate for doubling up of number of transistors on a chip which subsequently applies to the chip area as well. This law is not empirical

universal in nature of the kind of Gauss's law or Newton's laws of motion. It is one of the preliminary concepts in the area of integrated electronics that CMOS technology followed perfectly without fail for almost five decades. The real intention of Moore to propose the law was purely based on economical perspective since the technology process was too much costly as per the market index. The device imprint scaling makes it economical, but at the cost of exponentially growth in process complexity which tends to reduce the production yield. Silicon integrated electronics is an aggravated exposure of the human essence; whilst the Moore's law is all about economic considerations and human invention. The present demands of analog and digital industry make it economically not viable to scale silicon-based transistors any further. This has led to the demand for development of compound semiconductor material-based devices that not only outperform the generic Si based devices but also meet the stringent demands of modern-day analog and digital applications.

The spotlight of in-trend scientific and technological advancements achieved in the III-V compound semiconductor FETs with tailoring of device structures ranging from planar to vertical 3D designs are still faced by challenges to replace the generic CMOS completely. Predominantly, the challenge of integration of III-V devices into silicon is supposed to be the most important breakthrough in making III-V technology a success at commercial level. III- V semiconductors have been employed for couple of decades for high-frequency and high-speed transistors specifically for devices like HEMTSs, where the mobility of charge carriers is modulated using a hetero-structure [19]. However, there are some issues for HEMTs to be employed as low power digital devices due to high gate leakage current and hence is not the preferred device for scaling where gate leakage can affect more severely [20]. Although, HEMTs have been the basis of development of advanced III-V devices for applicability in modern day applications. Ternary semiconductor InGaAs has been recognized as highest transconductance ($\frac{\partial ID}{\partial VGS}$) HEMT [21]. There has been a substantial improvement in two important aspects of InGaAs MOSFETs that include gate stack and parasitic resistance. Gate oxide has a significant impact on gate control of the conduction channel. Parasitic resistance happens to occur in different forms that include the source/drain contact resistances, hetero junction barrier resistances, and extension region resistances. However, it is worth mentioning that parasitic resistance performance is much greater in generic MOSFETs as compared to III-V HEMTs. Technological advancements have pushed the scaling limit of In- GaAs MOSFET technology to as low as 10nm with challenges of parasitic resistance, gate stack and integration with silicon. A gate stack consists of a metallic gate with high-K oxide on top of the semiconductor channel, which regulates the electrostatic control of the gate over the conduction channel [22]. The determination a high-K gate stack requires an oxide shy of trapped charges and free of structural imperfections; forms a desirable oxide-semiconductor interface with considerable thermal conductivity. Interface charges result of an improper variable connection between the materials on two side of the interface. The gate oxide is scaled appropriately with an effective oxide thickness of less than 1 nm for superior electro- static gate-channel coupling. The advancements in silicon technology are disadvantageous in term of stable native oxide while as in III-V materials it causes Fermi-level extraction thereby difficult for gate to electrostatic integrity onto channel charges [23]. This leads to long term reliability issues in III-V based FETs. Considerable advancements have been made in recent past for improvement of oxide and compound semiconductor interface properties which revealed annealing and high temperature deposition techniques have significant effect on the interface properties such as atomic layer deposition [24]. A process termed as self-cleaning effect occurs where the native oxide gets removed preliminary to ALD. Buried channel approach employs InP as a barrier frame that has superior MOSFET performance, with posing limitations on scalability of effective oxide thickness [25]. Retaining high electron mobility in InGaAs

in MOS structures comprising of scaled gate oxide stacks is challenging due to coulomb's scattering, interface and phonon scattering that significantly affects the mobility of charge carriers.

Parasitic resistance is one of key challenges that determines the performance of MOS-FETs. The persistent efforts to reduce the ON-resistance in ultra-scaled III-V material based MOSFETs is still a challenging task. With low metal semiconductor resistance for ultra- scaled contacts, the Fermi level pinning takes place []. Recently developed contact- first approach of fabrication process proved to be an effective technique to significantly reduce the contact resistance as demonstrated for 200nm contacts [62]. Researchers are investigating other potential ways to limit the ON-resistance through silicide-based contacts with minimized temperatures which provides ease of process integration [69]. The designing of access region from source to channel forms a critical factor in determination of cumulative parasitic resistance of the device. The modern-day architectures of MOSFETs with reduced access resistance while maintaining high drive currents (transconductance) include gate-first, gate last FETs based on III-V materials with optimized etching and growth techniques [23].

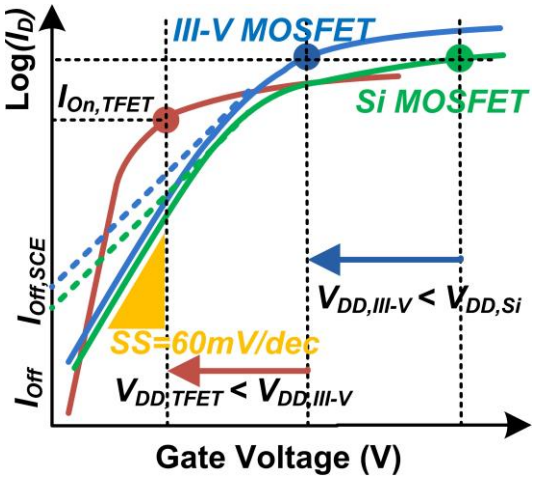


Figure 2: Comparison of transfer/input characteristics for III-V MOSFET, Si MOSFET and Tunnel FET. TFET has near to ideal subthreshold slope but suffers from limited drive current, while as Si MOSFET has subthreshold swing of 60mV/dec with enhanced drive current. The highest drive current is observed for III-V MOSFET, however with least subthreshold swing making it more suitable for high frequency and high-power switching applications.

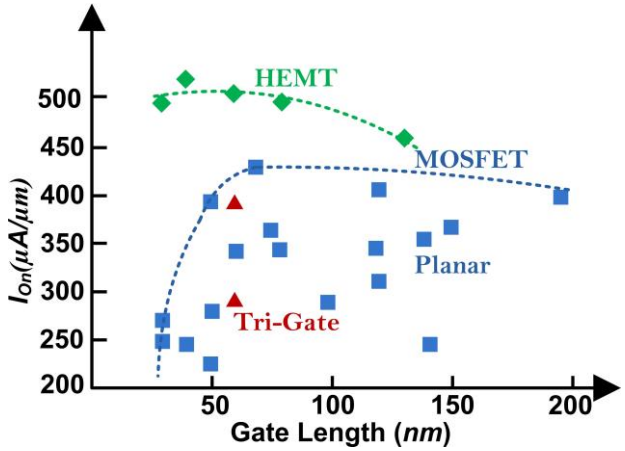


Figure 3: On state (drive) current for MOSFET, HEMT and tri-gate transistors for different gate lengths. As evident III-V HEMTs yield highest drive currents although with lower gate control in comparison to MOSFET and tri gate transistors.

Imbibition of new materials into CMOS technology process is accompanies by numerous challenges making the process even more complex. The problem with semiconductor market is that the requirement escalates much faster than the rate of development of technology. The performance of gallium nitride-based devices such as hetrerojunction Field-Effect Transistor is largely reliant on device scaling problems. Various simulation results reveal that a reduction in source to gate spacing length can significantly improvise the device performance, thereby increasing the device drive current and hence transconductance which simultaneously has a positive impact on gain of the device. On the similar context, the gate to drain spacing length do not pose a significant impact on device current-voltage characteristic performance. A number of published articles reveal that an increase in the Aluminium mole fraction of AlGaN buffer grounds the reduced device transconductance for both AlN/GaN/AlGaN hetrerojunction Field-Effect Transistors, and also increases the gate leakage current.

## 5. Conclusion

The scaling restraints requisite a transformation from planar architectures to three-dimensional device structures to cater future performance requirements of CMOS nodes beyond 10 nm. Compound semiconductor materials are progressively waged in various electronic, opto-electronic, and photonic applications due to the prospects of adjusting the properties over a broad parameter domain conveniently by tuning the alloy composition. Ironically, the material properties are also willed by the atomic-scale orientation of compound semiconductors in sub-nanometer scale. Compound semiconductors FET based logic circuits perform 5 folds faster than similar topology circuits based on silicon, whilst dissipating only half of the power. In this research a comprehensive review is presented that outlines how compound semiconductor materials mitigate various effects of aggressive scaling in nanometer scale and the adjoining effects.

## 6. Conflict of Interest

The authors have no conflict of interest.

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